What is claimed is:

1. A data processing apparatus comprising:

an address generation circuit generating a logical address for data including 10 bits of an imaginary part, 10 bits of a real part and 12 bits of a reserved part;

an address translation circuit translating the logical address into a physical address for data including 16 successive bits of the imaginary part and the real part;

a selection circuit generating a selection signal in response to the logical address;

a memory for storing 16 bits of data in accordance with the physical address and outputting the stored data;

a shifter receiving the data from the memory and shifting the received data in response to the selection signal;

an ALU processing an arithmetic operation in response to an output of the shifter and a processing result thereof; and

a mixing circuit mixing the data received from the memory and the processing result and outputting the mixed data to the memory.

2. A data processing apparatus according to claim 1, wherein a relationship between the physical address A and the logical address a is as follows:

$A = (a/2) + [(a/2)/4]$

wherein [x] means a Gaussian symbol signifying a maximum integer not exceeding x.

3. A data processing apparatus according to claim 1, wherein a relationship between a bit position B within the physical address and the logical address a is as follows:

$B = (a/2) - 4[(a/2)/4]$

wherein [x] means a Gaussian symbol signifying a maximum integer not exceeding x.

4. A data processing apparatus according to claim 1, wherein the memory including a plurality of memory blocks.

5. A data processing apparatus according to claim 1, wherein the mixing circuit includes a plurality of registers and a plurality of selectors operating in response to the select signal.

6. A data processing apparatus according to claim 5, wherein the resistors are 4 bit registers.

7. A method of accessing data comprising:

providing 32 bit data having a logical address a including 10 bits of an imaginary part, 10 bits of a real part and 12 bits of a reserved part;

deleting the reserved part;

serially storing the imaginary part and the real part into a memory having a 16 bit width; and

reading the stored data from the memory at an address A from the bit position B, both of which are designated as follows:

$A = (a/2) + [(a/2)/4]$

$B = (a/2) - 4[(a/2)/4]$

wherein [x] means a Gaussian symbol signifying a maximum integer not exceeding x.

8. A method of accessing data according to claim 7, wherein the 32 bit data including the imaginary part, the real part and the reserved part in that order.

9. A data processing apparatus comprising:

an address generation circuit generating a logical address for 32 bit width data including 10 bits of an imaginary part, 10 bits of a real part and 12 bits of a reserved part;

an address translation circuit translating the logical address into a physical address for data including 16 successive bits of the imaginary part and the real part;

a selection circuit generating a selection signal in response to the logical address;

a memory for storing 16 bit width data in accordance with the physical address and outputting the stored data;

a shifter receiving the data from the memory and shifting the received data in response to the selection signal;

an ALU processing an arithmetic operation in response to an output of the shifter and a processing result thereof;

an accumulator receiving the processing result and outputting the accumulated result; and

a mixing circuit mixing the data received from the memory and the accumulated result and outputting the mixed data to the memory.

10. A data processing apparatus according to claim 9, wherein a relationship between the physical address A and the logical address a is as follows:

$A = (a/2) + [(a/2)/4]$

wherein [x] means a Gaussian symbol signifying a maximum integer not exceeding x.

11. A data processing apparatus according to claim 9, wherein a relationship between a bit position B within the physical address and the logical address a is as follows:

$B = (a/2) - 4[(a/2)/4]$

wherein [x] means a Gaussian symbol signifying a maximum integer not exceeding x.

12. A data processing apparatus according to claim 9, wherein the memory including a plurality of memory blocks.

13. A data processing apparatus according to claim 9, wherein the mixing circuit includes a plurality of registers and a plurality of selectors operating in response to the select signal.

14. A data processing apparatus according to claim 13, wherein the resistors are 4 bit registers.

15. A data processing apparatus according to claim 13, wherein the registers including a first 12 bit register, a second 12 bit register and a 32 bit register.

16. A data processing apparatus according to claim 15, wherein the registers including a plurality of 4 bit registers.

17. A data processing apparatus according to claim 15, wherein the memory including a first memory for storing an odd address data and a second memory for storing an even address data.

18. A data processing apparatus according to claim 17, wherein the first 12 bit register receives data from the first memory, the second 12 bit register receives data from the second memory, and the 32 bit register receives data from the accumulator.